Patent Claims

- 1. A circuit arrangement for aircraft engine controllers for providing or generating a bipolar direct current output signal (I_{act}) as a function of at least one pulse-width modulated input signal (D, D*), comprising at least two driver stages (20, 21), each driver stage (20, 21) being activatable by a pulse-width modulated input signal (D, D*), and the or each driver stage (20, 21) being connected to preferably one step-down converter stage (22) in such a way that, when a first driver stage (21) is activated, a first switching element (T1, D1) of a step-down converter stage (22) activates a low-pass device (23) of the step-down converter stage (22), and, when a second driver stage (21) is activated, a second switching element (T2, D2) of the step-down converter stage (22).
- 2. The circuit arrangement as recited in Claim 1, characterized by two driver stages (20, 21), each of the two driver stages (20, 21) being activatable by a pulse-width modulated input signal (D, D*), and each of the two driver stages (20, 21) being connected to a step-down converter stage (22) in such a way that, when a first driver stage (20) is activated, the first switching element (T1, D1) of the step-down converter stage (22) activates the low-pass device (23) of the step-down converter stage (22), and, when the second driver stage (21) is activated, a second switching element (T2, D2) of the step-down converter stage (22) activates the low-pass device (23) of the step-down converter stage (22).
- 3. The circuit arrangement as recited in Claim 1 or 2, characterized in that each switching element of the step-down converter stage (22) has at least one transistor (T1, T2).
- 4. The circuit arrangement as recited in Claim 3, characterized in that a diode (D1, D2) cooperates with the transistor (T1, T2) of each switching element of the step-down converter stage (22).

- 5. The circuit arrangement as recited in one or more of Claims 2 through 4, characterized in that the low-pass device (23) of the step-down converter stage (22) has an inductor (L_{TP}) operating in pulsating operation.
- 6. The circuit arrangement as recited in one or more of Claims 2 through 5, characterized in that, when a positive output direct current signal (I_{act}) is to be provided by the circuit arrangement, the first driver stage (20) is activated by a pulse-width modulated input signal (D), while a permanent high-level signal acts upon the second driver stage (21), and that the first switching element (T1, D1) of the step-down converter stage (22) subsequently activates the low-pass device (23) of the step-down converter stage (22).
- 7. The circuit arrangement as recited in one or more of Claims 2 through 6, characterized in that, when a negative direct current output signal (I_{act}) is to be provided by the circuit arrangement, the second driver stage (21) is activated by a pulse-width modulated input signal (D*), while a permanent low-level signal acts upon the first driver stage (20), and that the second switching element (T2, D2) of the step-down converter stage (22) subsequently activates the low-pass device (23) of the step-down converter stage (22).
- 8. The circuit arrangement as recited in one or more of Claims 2 through 7, characterized in that the first switching element comprises a PNP transistor (T1) and the second switching element comprises an NPN transistor (T2), the base (B_{T1}) of the PNP transistor (T1) of the first switching element being connected to the first driver stage (20) and the base (B_{T2}) of the NPN transistor (T2) of the second switching element being connected to the second driver stage (21), the collector (C_{T1}) of the PNP transistor (T1) of the first switching element being connected to the collector (C_{T2}) of the NPN transistor (T2) of the second switching device, and the emitter (E_{T1}) of the PNP transistor (T1) of the first switching element being connected to a positive supply voltage terminal (+ U_{S}) and the emitter (E_{T2}) of the NPN transistor (T2) of the second switching element being connected to a negative supply voltage terminal (- U_{S}).
- 9. The circuit arrangement as recited in Claim 8, characterized in that a diode (D1), which cooperates with the PNP transistor (T1) of the first

switching element, is connected to the NPN transistor (T2) of the second switching element in such a way that the cathode (K_{D1}) of this diode (D1) is connected to the collector (C_{T2}) of the NPN transistor (T2) and the anode (A_{D1}) of this diode (D1) is connected to the emitter (E_{T2}) of the NPN transistor (T2).

- 10. The circuit arrangement as recited in Claim 8 or 9, characterized in that a diode (D2), which cooperates with the NPN transistor (T2) of the second switching element, is connected to the PNP transistor (T1) of the first switching element in such a way that the cathode (K_{D2}) of this diode (D2) is connected to the emitter (E_{T1}) of the PNP transistor (T1) and the anode (A_{D2}) of this diode (D2) is connected to the collector (E_{T1}) [sic; C_{T1}] of the PNP transistor (T1).
- 11. The circuit arrangement as recited in Claim 8, 9, or 10, characterized in that the cathode (K_{D1}) of the diode (D1), which cooperates with the PNP transistor (T1) of the first switching element, is connected to the collector (C_{T1}) of the PNP transistor (T1) of the first switching element and that the anode (A_{D2}) of the diode (D2), which cooperates with the NPN transistor (T2) of the second switching element, is connected to the collector (C_{T2}) of the NPN transistor (T2) of the second switching element.
- 12. The circuit arrangement as recited in Claim 8, 9, or 10, characterized in that each driver stage (20, 21) has a transistor (Q1, Q2) and resistors (R1 through R14) and capacitors (C1 through C4) which are connected to the transistor.